CLAIMS

WHAT IS CLAIMED:

1. A method of forming a barrier layer in an interconnect structure formed on a substrate, the method comprising:

adjusting a direction of target atoms in a deposition ambient by ionizing a fraction of said target atoms, and applying a bias voltage to said interconnect structure so as to predominantly deposit target ions on a bottom surface of said interconnect structure to form a bottom barrier layer;

changing a composition of said deposition ambient while reducing said bias voltage to deposit a second barrier layer on sidewalls of said interconnect structure;

substantially re-establishing said deposition ambient; and

conformally depositing target atoms to form a third barrier layer over said bottom barrier layer and said second barrier layer.

2. The method of claim 1, wherein said deposition ambient comprises tantalum.

3. The method of claim 1, wherein at least a fraction of said target atoms is liberated from a sputter target.

4. The method of claim 1, wherein adjusting a direction of said target atoms further includes controlling a pressure of a deposition atmosphere surrounding said target and said substrate.

5. The method of claim 1, wherein adjusting a direction of said target atoms further includes controlling at least one of a substrate temperature and geometry factor during the deposition of said target atoms.

6. The method of claim 1, wherein said bias voltage is applied for approximately 1-5 seconds.

7. The method of claim 6, wherein a thickness of said bottom barrier layer is in the range of approximately 1-5 nm.

8. The method of claim 1, further comprising re-sputtering a portion of said second barrier layer prior to depositing said third barrier layer.

9. The method of claim 1, further comprising determining an amount of said bias voltage for a specified deposition tool and a given set of process parameters prior to adjusting the direction of said target atoms.

10. The method of claim 9, wherein said process parameters include at least one of a pressure of said deposition ambient, a temperature of said substrate, an ionization power for ionizing said target atoms and a magnetic field prevailing in said deposition ambient.

11. The method of claim 1, wherein said deposition ambient is changed by adding nitrogen.

12. The method of claim 1, wherein said interconnect structure includes a trench and a via formed therein, and said method further comprises re-sputtering a portion of material of said bottom barrier layer prior to forming said second barrier layer.

13. A method of forming a tantalum-based barrier layer, the method comprising:

depositing tantalum by ionizing physical vapor deposition primarily at a bottom surface of a via formed in a dielectric layer of a metallization structure; and

depositing a tantalum nitride/tantalum bi-layer on sidewalls of said via.

14. The method of claim 13, wherein said physical vapor deposition includes applying a bias voltage to said metallization structure to direct tantalum atoms liberated from a sputter target substantially perpendicularly to said bottom surface.

15. The method of claim 14, further including controlling a pressure of a deposition atmosphere during said physical vapor deposition.

16. The method of claim 14, further including controlling at least one of a substrate temperature and geometry factor during the physical vapor deposition.

17. The method of claim 14, wherein said bias voltage is applied for approximately 1-5 seconds.

18. The method of claim 13, wherein a bottom barrier layer is formed during the physical vapor deposition and a thickness of said bottom barrier layer is in the range of approximately 1-5 nm.

19. The method of claim 13, further comprising re-sputtering a portion of the tantalum atoms prior to depositing a tantalum nitride/tantalum bi-layer.

20. The method of claim 14, further comprising determining an amount of said bias voltage for a specified deposition tool and a given set of process parameters prior to depositing tantalum ions.

21. The method of claim 20, wherein said process parameters include at least one of a pressure of said deposition ambient, a temperature of said metallization structure, an ionization power for ionizing said tantalum atoms and a magnetic field prevailing in said deposition ambient.

22. The method of claim 13, wherein said tantalum nitride/tantalum bi-layer is deposited by ionized physical vapor deposition.

23. The method of claim 13, wherein said tantalum ions and said tantalum nitride/tantalum bi-layer are deposited in a common process chamber without breaking a vacuum established therein.

24. The method of clam 13, wherein said metallization structure includes a trench and a via formed therein, and said method further comprises re-sputtering a portion of tantalum atoms deposited on a bottom surface of said trench prior to depositing said tantalum nitride/tantalum bi-layer.

25. A metallization structure in an integrated circuit, comprising:

a first metal region formed in a first dielectric layer;

a second metal region formed above said first metal region in a second dielectric layer; and

a barrier layer stack including a first sub-layer and a second sub-layer and separating said second metal region from said second dielectric layer and said first metal region, wherein said first sub-layer is in contact with said second dielectric layer, and said second sub-layer is in contact with said first metal region.

26. The metallization structure of claim 25, wherein a material of said second sub-layer has a greater adhesion to the metal of said first metal region than a material of said second sub-layer.

27. The metallization structure of claim 26, wherein said first sub-layer comprises tantalum nitride and said second sub-layer comprises tantalum.

28. The metallization structure of claim 27, further comprising a tantalum layer formed over said first sub-layer and in contact with said second metal region.